Remarks/Arguments:

Claims 17-21 are pending and rejected in the application. Claim 17 and 19 have been amended. No new matter has been added.

On page 2 of the Official Action, the Examiner states that he understands that Applicants' invention has two different memories with two different devices. However, the Examiner also states that independent claims 17 and 19 do not indicate that there is a difference between the two memories. Thus, the Examiner is interpreting the volatile buffer memory of the drive device as being the same as the non-volatile memory of the control device. Applicants have therefore amended claims 17 and 19 to clarify that the drive device and a control device are two different memories having two different memories connected through a bus.

On page 2, the Official Action rejects claims 17-21 under 35 U.S.C. § 102(b) as being anticipated by Tadayuki (JP 8-329469). It is respectfully submitted, however, that the claims are patentable over the art of record for at least the reasons set forth below.

Applicants invention, as recited by claim 17, includes features which are neither disclosed nor suggested by the art of record, namely:

a drive device housing and optical disk;

a control device connected to said drive device; and

a bus through which said control device is connected to said drive device, wherein

said drive device has:

a volatile buffer memory; ...

...said control device has:

a memory; ...

Claim 17 relates to a drive device which has a volatile buffer memory and a control device which has a memory (two different devices having two different memories). Specifically,

the drive device and control device are connected to each other through a bus. A transmitting unit of the control device transmits information for adjustment to the drive device. The adjustment information stored in memory of the control device is maintained in the memory unless the supply of power to the control device is suspended. Support for these features are at least shown in Fig. 2 and described on pages 16-26 of Applicants' specification. No new matter has been added.

On page 3, the Official Action states that Tadayuki's memory 47 is the same as both the volatile buffer memory of Applicants' drive device and the memory of Applicants' control device. Thus, the Examiner is interpreting Tadayuki's memory 47 as both the memories and the Applicants' drive device and the memory in Applicants' control device. Applicants' drive device and control device, however, have two different memories which are connected through a bus (see amendments to claims 17 and 19). Thus, Tadayuki is deficient in suggesting two different memories in two different devices as currently recited in Applicants' claims 17 and 19.

Applicants' claim 17 is different than the art of record because of two different devices (drive device 110 and control device 100 which are connected through a bus) which have two different memories respectively (a volatile buffer memory 112 and memory 102). Furthermore, claim 17 is different than the art of record because information for adjustment processing is maintained in the memory of the control device unless the power supply to the control device is suspended. In general, when the volatile buffer memory of the drive deice is erased, the control device having the memory may then update the volatile buffer memory ("*... a drive device housing and optical disk; a control device connected to said drive device; and a bus through which said control device is connected to said drive device, wherein said drive device has a volatile buffer memory; ... said control device has a memory; ...*").

As shown in Applicants' Fig. 2, drive device 100 includes a buffer memory 112, and control device 100 includes a non-volatile memory 102. When power is suspended to drive device 110, the volatile buffer memory 112 is erased. The buffer memory 102 of the control device, however, is not erased (unless power supplied to the control device is suspended). This allows the erased volatile buffer memory 112 to be updated based on the adjustment information stored in memory 102. Thus, as shown in Fig. 2, the adjustment information stored in memory 102 is transmitted from the control device 100 to drive device 110 through bus 115.

This feature is at least supported on page 15, lines 5-10, page 19, lines 1-15, and page 25, line 10, to page 26, line 10, of the specification ("*disk recorder 100 ... is connected to an optical disk drive 110 through a serial bus 115 ... drive controller 123 transmits the recording and replaying conditions 222 ... to the optical disk drive 110, and the optical disk drive 110 sets the received recording and replaying conditions 222 in the ... storage buffer 112 ... supply of electric power to said information storage buffer 102 is not stopped unless supply of power to the optical disk recorder itself is stopped, and the stored recording and replaying conditions are maintained even in the standby state*").

Thus, since Tadayuki does not suggest a memory in a control device and a volatile buffer memory in a drive device which are connected through a bus, claim 17 is patentable over the art of record.

Claim 19 has similar features to claim 17. Thus, claim 19 is also patentable over the art of record for at least the reasons set forth above.

Dependent claims 18, 20 and 21 include all the features of the claims from which they depend. Thus, these claims are also patentable over the art of record for at least the reasons set forth above with respect to claims 17 and 19.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Respectfully submitted,

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